1. A method of preparing a wafer for integrated circuit fabrication comprising:

providing a bulk silicon substrate;

depositing a carbon-doped silicon layer on said bulk silicon substrate; and growing an epitaxial silicon layer overlying said carbon-doped silicon layer to provide a starting wafer for integrated circuit fabrication.

2. The method according to Claim 1 wherein said carbon-doped silicon layer is deposited by reduced pressure chemical vapor deposition.

3. The method according to Claim 1 wherein said carbon-doped silicon layer has a thickness of between about 100 and 200 Angstroms.

4. The method according to Claim 1 wherein said carbon-doped silicon layer has a carbon content of up to 0.5%.

5. The method according to Claim 1 wherein said epitaxial silicon layer has a thickness of between about 300 and 400 Angstroms.

6. A method of fabricating an integrated circuit device comprising:

providing a bulk silicon substrate;

depositing a carbon-doped silicon layer on said bulk silicon substrate;

growing an epitaxial silicon layer overlying said carbon-doped silicon layer to provide a starting wafer for said integrated circuit device fabrication; and

fabricating said integrated circuit device on said starting wafer by the steps comprising:

forming a gate electrode on said starting wafer;

implanting LDD and source and drain regions in said starting wafer adjacent to said gate electrode; and

implanting a heavy ion to form halo implants adjacent to said LDD regions and underlying said gate electrode wherein said halo implants extend to an interface between said epitaxial silicon layer and said carbon-doped silicon layer.

7. The method according to Claim 6 wherein said carbon-doped silicon layer is deposited by chemical vapor deposition.

8. The method according to Claim 6 wherein said carbon-doped silicon layer is deposited by reduced pressure chemical vapor deposition.

9. The method according to Claim 6 wherein said carbon-doped silicon layer has a thickness of between about 100 and 700 Angstroms.

10. The method according to Claim 6 wherein said carbon-doped silicon layer has a carbon content of up to 0.5%.

11. The method according to Claim 6 wherein said epitaxial silicon layer has a thickness of between about 300 and 500 Angstroms.

12. The method according to Claim 6 wherein carbon ions in said carbon-doped silicon layer act as a silicon interstitial sink for silicon interstitials formed by said halo implants to prevent end of range secondary defect formation.

13. The method according to Claim 6 wherein said heavy ions comprise antimony or indium.

14. A method of fabricating an integrated circuit device comprising:

providing a bulk silicon substrate;

depositing a carbon-doped silicon layer on said bulk silicon substrate;

growing an epitaxial silicon layer overlying said carbon-doped silicon layer to provide a starting wafer for said integrated circuit device fabrication; and

fabricating said integrated circuit device on said starting wafer by the steps comprising:

forming a gate electrode on said starting wafer;

implanting LDD and source and drain regions in said starting wafer adjacent to said gate electrode; and

implanting heavy ions to form halo implants adjacent to said LDD regions and underlying said gate electrode wherein said halo implants extend to an interface between said epitaxial silicon layer and said carbon-doped silicon layer wherein carbon ions in said carbon-doped silicon layer act as a silicon interstitial sink for silicon interstitials formed by said halo implants to prevent end of range secondary defect formation.

15. The method according to Claim 14 wherein said carbon-doped silicon layer is deposited by reduced pressure chemical vapor deposition.

16. The method according to Claim 14 wherein said carbon-doped silicon layer has a thickness of between about 100 and 700 Angstroms.

17. The method according to Claim 14 wherein said carbon-doped silicon layer has a carbon content of up to 0.5%.

18. The method according to Claim 14 wherein said epitaxial silicon layer has a thickness of between about 300 and 500 Angstroms.

19. The method according to Claim 14 wherein said heavy ions comprise antimony or indium.

20. An integrated circuit device comprising:

a starting wafer comprising:

a bulk silicon substrate;

a carbon-doped silicon layer overlying said bulk silicon substrate; and

an epitaxial silicon layer overlying said carbon-doped silicon layer;

a gate electrode on said starting wafer;

LDD and source and drain regions in said starting wafer adjacent to said gate electrode; and

heavy ion halo implants adjacent to said LDD regions and underlying said gate electrode wherein said halo implants extend to an interface between said epitaxial silicon layer and said carbon-doped silicon layer wherein carbon ions in said carbon-doped silicon layer act as a

silicon interstitial sink for silicon interstitials formed by said halo implants to prevent end of range secondary defect formation.

21. The device according to Claim 20 wherein said carbon-doped silicon layer is deposited by reduced pressure chemical vapor deposition.

22. The device according to Claim 20 wherein said carbon-doped silicon layer has a thickness of between about 100 and 700 Angstroms.

23. The device according to Claim 20 wherein said carbon-doped silicon layer has a carbon content of up to 0.5%.

24. The device according to Claim 20 wherein said epitaxial silicon layer has a thickness of between about 300 and 500 Angstroms.

25. The device according to Claim 20 wherein said heavy ions comprise antimony or indium.